WHAT IS CLAIMED:

1. A flash memory comprising:

a local row decoder circuit configured to drive word lines coupled to a bank of a flash memory responsive to separate read and write control signals provided thereto from outside the local row decoder circuit.

2. A flash memory according to Claim 1 wherein the flash memory supports read-while-write capability wherein a read operation in a first bank of the flash memory can be carried out simultaneous with a write operation in a second bank of the flash memory.

3. A flash memory according to Claim 1 further comprising:

a global row decoder circuit, coupled to the local row decoder circuit via the separate read and write control signals, and configured to activate the separate read and write control signals based on an address provided to the global row decoder circuit that indicates memory cells associated with the address are accessed using the word lines.

4. A flash memory according to Claim 3 wherein the local row decoder circuit comprises a first local row decoder circuit, the bank comprises a first bank, and the word lines comprise first word lines, the flash memory further comprising:

a second local row decoder circuit configured to drive a second bank of the flash memory, separate from the first bank, via second word lines that are separate from the first word lines, wherein the second local row decoder circuit is coupled to the global decoder circuit by the separate read and write control signals.

5. A flash memory according to Claim 4 wherein the global row decoder circuit is configured to activate the first and second local row decoder circuits using the separate read and write control signals.

6. A flash memory according to Claim 3 wherein the local row decoder circuit and the global row decoder circuit are spaced apart within the flash memory.

7. A flash memory according to Claim 4 wherein the global row decoder circuit comprises:

a read address decoder circuit configured to activate the read control signal coupled to the first and second separate banks based on a read address provided thereto; and

a write address decoder circuit configured to activate the write control signal coupled to the first and second separate banks based on a write address provided thereto.

8. A flash memory according to Claim 3 wherein the local row decoder circuit comprises first and second bank select circuits configured to pass the separate read and write control signals to a plurality of word line drivers coupled to a sector within the bank.

9. A flash memory according to Claim 8 wherein the first and second bank select circuits comprise at least one totem-pole arrangement of first and second transistors wherein the first and second transistors are conductive to pass at least one of the separate read and write control signals to the plurality of word line drivers associated with the sector responsive to at least one select signal that indicates the local row decoder circuit is coupled to the bank that includes a memory location corresponding to a write or read address provided to the global decoder circuit.

10. A flash memory according to Claim 8 wherein the first and second bank select circuits comprise at least one pass transistor configured to pass at least one of the separate read and write control signals to the plurality of word line drivers responsive to at least one bank select signal that indicates that the bank to which the local row decoder circuit is coupled includes a memory location corresponding to an address provided to the flash memory.

11. A flash memory according to Claim 3 wherein the global row decoder circuit comprises first and second NAND combinatorial logic circuits or first and second NOR combinatorial logic circuits configured to provide the separate read and write control signals.

12. A flash memory according to Claim 11 wherein the first and second NAND combinatorial logic circuits or the first and second NOR combinatorial logic circuits are configured to activate responsive to a read address for a read operation or a write address for a write operation respectively.

13. A flash memory according to Claim 1 wherein the bank of flash memory comprises a first bank of the flash memory configured to perform a write operation addressed to the first bank via the local row decoder circuit, the flash memory further comprising:

a second bank of the flash memory configured to perform a read operation addressed thereto via a second local row decoder circuit simultaneous with the write operation.

14. A flash memory according to Claim 3 wherein the bank comprises a first bank, wherein the flash memory has read-while-write capability comprising an ability to perform a write operation in the first bank of the flash memory via the first local row decoder circuit while simultaneously performing a read operation in a second bank of the flash memory via another local row decoder circuit.

15. A flash memory according to Claim 3 wherein the flash memory has read-while-write capability comprising an ability to perform a first read or write operation in a first sector of the bank while simultaneously performing a second read or write operation in a second sector of the bank that is separate from the first sector via another local row decoder circuit.

16. A flash memory having read-while-write capability comprising:

a plurality of banks of a flash memory;

a plurality of local row decoder circuits configured to drive a plurality of word lines coupled to a respective sector in each of the plurality of banks; and

a global row decoder circuit configured to provide separate write and read control signals to each of the plurality of local row decoder circuits to enable a read operation in a first sector in one of the plurality of banks and enable a write operation in a second sector in another of the plurality of banks simultaneous with the read operation.

17. A flash memory according to Claim 16 wherein the global row decoder circuit is coupled to the plurality of local row decoder circuits via the separate read and write control signals, and configured to determine whether to activate the separate read and write control signals based on an address for the read or write operation provided to the global row decoder circuit.

18. A flash memory according to Claim 16 wherein the plurality of local row decoder circuits and the global row decoder circuit are spaced apart within the flash memory.

19. A flash memory according to Claim 17 wherein the global row decoder circuit comprises:

a read address decoder circuit configured to activate the read control signal coupled to the first and second separate banks based on a read address provided thereto; and

a write address decoder circuit configured to activate the write control signal coupled to the first and second separate banks based on a write address provided thereto.

20. A flash memory according to Claim 19 wherein the read address decoder circuit and the write address decoder circuit are configured to be active simultaneously.

21. A flash memory according to Claim 16 wherein the local row decoder circuit comprises first and second bank select circuits configured to pass the separate read and write control signals to a plurality of word line drivers coupled to a sector within the bank.

22. A flash memory according to Claim 21 wherein the first and second bank select circuits comprise at least one totem-pole arrangement of first and second transistors wherein the first and second transistors are conductive to pass at least one of the separate read and write control signals to the plurality of word line drivers associated with the sector responsive to at least one select signal that indicates the

local row decoder circuit is coupled to the bank that includes a memory location corresponding to a write or read address provided to the global decoder circuit.

23. A flash memory according to Claim 21 wherein the first and second bank select circuits comprise at least one pass transistor configured to pass at least one of the separate read and write control signals to the plurality of word line drivers responsive to at least one bank select signal that indicates that the bank to which the local row decoder circuit is coupled includes a memory location corresponding to an address provided to the flash memory.

24. A flash memory according to Claim 18 wherein the global row decoder circuit comprises first and second NAND combinatorial logic circuits or first and second NOR combinatorial logic circuits configured to provide the separate read and write control signals.

25. A flash memory according to Claim 24 wherein the first and second NAND combinatorial logic circuits or the first and second NOR combinatorial logic circuits are configured to activate responsive to a read address for a read operation or a write address for a write operation respectively.

26. A flash memory according to Claim 16 wherein the bank of flash memory comprises a first bank of the flash memory configured to perform a write operation addressed to the first bank via the local row decoder circuit, the flash memory further comprising:

a second bank of the flash memory configured to perform a read operation addressed thereto via a second local row decoder circuit simultaneous with the write operation.

27. A flash memory according to Claim 17 wherein the bank comprises a first bank, wherein the flash memory has read-while-write capability comprising an ability to perform a write operation in the first bank of the flash memory via the first local row decoder circuit while simultaneously performing a read operation in a second bank of the flash memory via another local row decoder circuit.

28. A flash memory according to Claim 17 wherein the flash memory has read-while-write capability comprising an ability to perform a first read or write operation in a first sector of the bank while simultaneously performing a second read or write operation in a second sector of the bank that is separate from the first sector via another local row decoder circuit.